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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/773,522
Filing Date: February 06, 2004
Appellant(s): HUANG ET AL.

Kent J. Tobin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 15, 2008 appealing from the Office action mailed September 13, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,372,580	Shiau	4-2002
6,847,087	Yang et al.	1-2005
2004/0262650	Iwata et al.	12-2004
5,506,160	Chang	4-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiau (US Pat. 6,372,580) in view of Yang et al. (US Pat. 6,847,087, hereinafter Yang).

Regarding claim 1, Shiau teach a method for manufacturing ROM memory devices in figure 4 and figures 5A-11 D, the method comprising:

• forming a cell region as an array region for ROM memory devices (figure 4), the array including containing continuous bit line regions BN+ in each cell (the bit lines BN+ are formed in figures 6A-6D);

• forming a gate structure POLY within the cell region (figures 9A-9D);

• forming a first sidewall spacer 47 overlying a first side of the gate structure POLY and a second sidewall spacer 47 overlying a second side of the gate structure POLY (figures 10B and 10D, column 4 lines 47-48), each sidewall spacer extends over and overlaps a portion of source/drain regions BN+ (as in the instant application, the source/drain regions are a part of the

bit lines BN+), the first and second sidewall spacer 47 also adapted to separate the gate structure POLY from the source/drain regions BN+;

• applying a refractory metal overlying the entire substrate including the gate structure POLY including the first and second sidewall spacers 47 (column 4 line • 56 through column 5 line 4);

• heat treating to form silicide regions 51 overlying the gate structure POLY and exposed portions of the source/drain regions BN÷ (it is noted that Shiau does not explicitly state their heat treatment resulting in "alloying" the refractory metal; nonetheless, this is implicitly taught by Shiau as alloying is inherent in heat treating to form the silicide; that is, the silicon and the metal inherently alloy together in forming the silicide)

• and selectively removing the refractory metal layer from the sidewall spacers (figures 11A-11D and column 4 line 56 through column 5 line 4; note that the refractory metal layer is removed from 'all sections where it did not form an alloy, that is all section except for where the refractory metal contacted the polysilicon gate and silicon substrate directly).

Shiau does not teach forming a trench isolation structure within a cell region of the substrate. Since Shiau does not teach forming the isolation structure, Shiau also does not teach the claimed features and arrangement of the isolation structure and its structural arrangement.

Yang teaches in figures 2(a)-2(c) a ROM memory array which includes continuous bit lines (SPWI/SPW2/SPW3) and gate structures (M0~M15) extending over and perpendicular to the bit lines. Yang also teaches a shallow trench isolation structure (STI) within a cell region.

The shallow trench isolation structure, as seen in figures 2(b) and 2(c), are provided between adjacent bit lines extending in the same direction as the bit lines to isolate adjacent bit lines

Shiau and Yang are from the same field of endeavor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to employ the trench isolation structures of Yang in the method and device of Shiau. The motivation for doing so is to isolate the bit lines from each other (Yang column 4 lines 44-47). Therefore, it would have been obvious to combine Shiau with Yang to obtain the invention of claim 1.

In combining the trench isolation regions of Yang into the method and device of Shiau, the resulting method renders claim 1 obvious. In the combination, the trench isolation structure will separate a continuous bit line region of the cell from another bit line region from another cell, the sidewall spacers will extend over and overlap a portion of the trench isolation structure, and the trench isolation structure will be separated from the gate structure by the sidewall spacers. Further, since the refractory metal layer of Shiau is applied over the entire substrate surface, it will be applied over an exposed portion of the trench isolation structure and the refractory metal will be selectively removed from the exposed surface of the trench isolation structure since it will not alloy to form the silicide on this portion:

Regarding claim 2, the refractory metal layer of Shiau is titanium or cobalt (column 4 line 56).

Regarding claim 3, the trench isolation region of Yang is an STI region (figure 2(b)).

Regarding claim 4, it is obvious to one or ordinary skill in the art at the time of the invention that the STI region comprises silicon dioxide since silicon dioxide is a commonly used material for filling trenches in STI applications.

Regarding claim 6, the first and second sidewall spacers of Shiau are a dielectric material (column 4 line 52).

Regarding claim 7, the buried bit line structure of Shiau is within the source/drain region.

Regarding claim 8, the trench isolation STI is within the substrate at a predetermined depth which is greater than a junction depth of the buried bit line SPW (Yang, column 4 lines 48-51).

Claims 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiau with Yang as applied to claims 1-4 and 6-8 above, and further in view of Iwata et al. (US 2004/0262650 A1).

Liu with Shiau do not explicitly disclose a channel region using a length of about 0.25 micron and less or the gate structure having a width of 0.25 micron and less. Iwata et al. teach semiconductor devices. Iwata et al. teach in paragraph 3 that recently the integration level of semiconductor devices is becoming higher and higher and thus there is a demand for smaller elements. Iwata et al. teach in paragraph 24 that the gate electrode (gate structure) is formed to a width of 100 nm (0.1 micron). It is noted that this paragraph relates to figure 44, which shows that channel length as the same as the gate width, thus Iwata teach both the gate structure and channel length of less than 0.25 micron.

Shiau with Yang and Iwata et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to form the gate structure width and channel length to 0.25 micron or less. The motivation for

doing so is to meet the demand for smaller elements for higher integration. Therefore, it would have been obvious to combine Shiau and Yang with Iwata et al. to obtain the invention of claims 5 and 9.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiau with Yang as applied to claims 1-4 and 6-8 above, and further in view of Chang (US Patent No. 5,506,160).

Shiau and Yang each teach an array of ROM cells (see figure 3A of Liu and figure 4 of Shiau, for example) but do not explicitly disclose their array having at least eight cells by eight cells. Nonetheless, it is considered obvious to form a ROM array to have at least eight cells by eight cells. Each cell represents one bit of data. Chang teach a ROM array in figure 5, for example. Chang et al. teach forming the array to be a 64 Mbit array. As one of ordinary skill in the art would recognize, a 64 Mbit array has at least eight cells by eight cells. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the array of Shiau with Yang to have at least eight cells by eight cells. The motivation for doing so is to meet an industry need of higher integration and larger memory arrays and to provide a greater amount of memory needed for modern electronics devices. Thus, it would have been obvious to form the array to at least eight cells by eight cells as claimed.

(10) Response to Argument

A. Rejection of claims as obvious over the Shiau Patent in view of the Yang Patent

Appellant argues that "in order to establish a prima facie case of obviousness, there must be some suggestion in either the references themselves or in the knowledge generally available to

one of ordinary skill in the art, to modify the reference or combine reference teachings". In response, the Examiner notes that the above rejection clearly established the motivation or suggestion to combine the references. The stated motivation came directly from the Yang reference. In fact, the examiner specifically pointed to the portion of the Yang patent (column 4 lines 44-47) which provides the motivation to include the trench isolation structure taught by Yang into the device of Shiau (to isolate adjacent buried bit lines).

Appellant further argues that "there is no suggestion in the Shiau Patent that would motivate one of ordinary skill in the art to combine it with the Yang Patent". However, there is no requirement that the motivation to combine the references must come from the primary reference, in this case Shiau. As established above, the motivation to combine the references came directly from the secondary reference (Yang).

Appellant additionally argues:

"Specifically, an object of the Shiau Patent is the development of a silicide layer to reduce the electrical resistance in the word and bit lines"... "By contrast, as shown in Figure 2(a) (reproduced below) of the Yang Patent, this reference utilizes a contact plug (102) which penetrates the surface of the drain region and buried bit lines in order to short-circuit the drain and bit lines:".... "Accordingly, use of the salicide process and the formation of a silicide layer as taught in the Shiau Patent, in combination with the Yang Patent, would be nonsensical. Specifically, the silicide layer of the Shiau Patent is used to decrease electrical resistance of the drain and bit line region, while the contact plug of the Yang Patent is electrically coupled to short-circuit this region. In view of this conflicting function, use of the contact plug of the Yang Patent is plainly inconsistent with the expressed objective of the Shiau Patent."

However, at no point did the above rejection suggest combining the silicide layer of the Shiau patent with the device of the Yang patent. The Yang patent was relied upon solely for the teaching of a trench isolation structure between adjacent buried bit lines. The Shiau patent

teaches all the limitations of independent claim 1 except the trench isolation structure. The Yang patent teaches a trench isolation structure in a similar device, and provides a motivation for using this isolation structure. Therefore, whether or not the silicide layer of Shiau can be combined with the device of Yang is moot. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Appellant again argues that "the Examiner is respectfully reminded that any suggestion to combine references must be found in the prior art, and not be based upon applicant's own disclosure". As stated above, the suggestion to combine the references in the manner set forth in the rejection came directly from the Yang patent, and therefore was not based on Appellant's own disclosure. Further, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Appellant further argues "claims 2-10 which depend upon claim 1 should also be patentable based on the same rationale as discussed for claim 1". However, the combination of the Shiau and Yang patents teaches all the limitations of underlying claim 1, and the Yang patent explicitly provides a motivation for combining the references in the manner suggested by the Examiner. For this reason and for the reasons set forth above in response to Appellant's

arguments, claim 1 is not patentable. Therefore, dependent claims 2-10 are not patentable based on their dependence from claim 1 and for the reasons set forth in the above rejection.

B. Rejection of Claims as obvious over the Shiau and Yang Patents Further in Combination with the Iwata Publication

Appellant argues that "Iwata Publication does not appear to disclose the continuous extension of the bit line portion underneath a gate structure in the manner of the claimed embodiments". The Examiner could not find this allegedly missing limitation in any of the pending claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The Shiau and Yang patents, in combination, teach all elements of claim 1. Iwata was merely relied upon to teach the specific dimensional requirements of claims 5 and 9.

C. Rejection of Claims as obvious over the Shiau and Yang Patents Further in Combination with the Chang Patent

Appellant argues that "Chang Patent does not appear to disclose the formation of sidewall spacers separating a gate from trench isolation structures". As indicated in the above rejection, the combination of the Shiau and Yang patents teaches all limitations of claim 1, including sidewall spacers separating a gate from trench isolation structures. The Chang patent was merely relied upon for the teaching of an array having at least eight cells by eight cells, as required by claim 10. Therefore, Appellant's argument regarding the Chang patent is moot.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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